Exhibit 2

Exhibit B-1
ACQIS's Preliminary Infringement Contentions for U.S. Patent No. 9,529,768
Microsoft Xbox One

The chart below identifies where each element of the asserted claims of U.S. Patent No. 9,529,768 ("'768 patent") is found in the Microsoft Xbox One series console (all models, including the original Xbox One (including but not limited to the 1520 and 1540 models), Xbox One S (including but not limited to the 1681 model), and Xbox One X (including but not limited to the 1787 model), are accused and are collectively referred to herein as "Xbox One" and "Accused Xbox One Products"). ACQIS contends that all Xbox One series consoles made, used, tested, offered for sale, sold, or imported into the United States by Microsoft, that share the features detailed below with reference to various exemplary Xbox One models, infringed at least claims 1, 2, 13, and 17 of the '768 patent in the manner charted herein. Specifically, all Xbox One series consoles that include PCIe functionality infringed as set forth below.

This chart contains evidence relating to various Xbox One models, including the original Xbox One, Xbox One S, and Xbox One X. The features of these products that are relevant to infringement are common across Xbox One models. The Accused Xbox One Products are not limited to these products, and ACQIS reserves the right to identify additional products based on information obtained in discovery.

ACQIS's contentions are not limited to the PCIe implementations discussed below. ACQIS does not possess information regarding the specific manner in which all of the Accused Xbox One Products utilize PCIe functionality, beyond the uses discussed below. ACQIS contends that all implementations of PCIe in the Accused Xbox One Products infringed for the reasons set forth herein. ACQIS reserves the right to supplement and/or amend its contentions to provide further specificity based on information obtained in discovery.

Claim Language	**Infringement Evidence**
1. A computer, comprising:	The Xbox One is a computer running a modified Hyper-V hypervisor as its host operating system and two partitions: Xbox OS, which runs games, and an OS based on Windows, which runs apps. https://www.extremetech.com/gaming/156467-xbox-one-hardware-and-software-specs-detailed-and-analyzed.

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Claim Language	Infringement Evidence
	 https://en.wikipedia.org/wiki/Xbox_One#/media/File:Microsoft-Xbox-One-Console-Set-wKinect.jpg.

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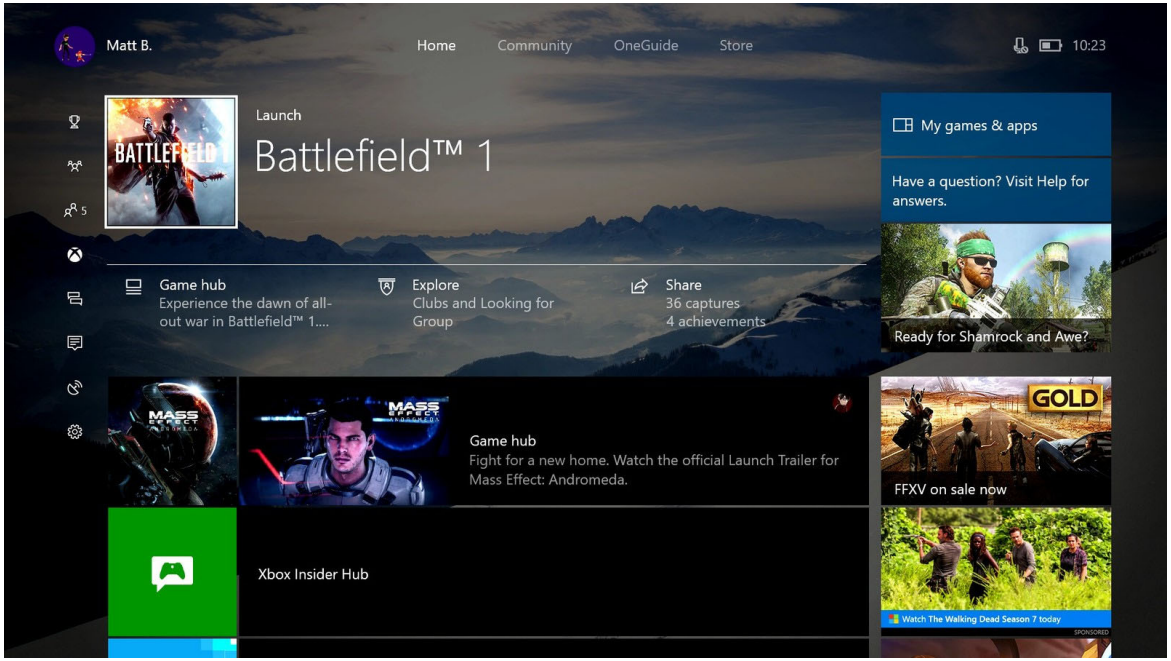
Claim Language	Infringement Evidence
	 https://www.windowscentral.com/evolution-xbox-one-dashboard-ui.
[1.a] an integrated central processing unit, interface controller and Phase-Locked Loop (PLL) clock circuitry in a single chip;	The Xbox One contains an integrated central processing unit, interface controller and Phase-Locked Loop (PLL) clock circuitry in a single chip. The Xbox One includes a single-chip, semi-custom processor (i.e., Accelerated Processor Unit (APU)), e.g., the X887732-001 shown below, consisting of a CPU and GPU integrated on a single chip. All eight CPU cores and the GPU are on the same die.

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	 Teardown photograph of processor chip from Xbox One. The processor chip is labeled "Main SoC" in the block diagram below.

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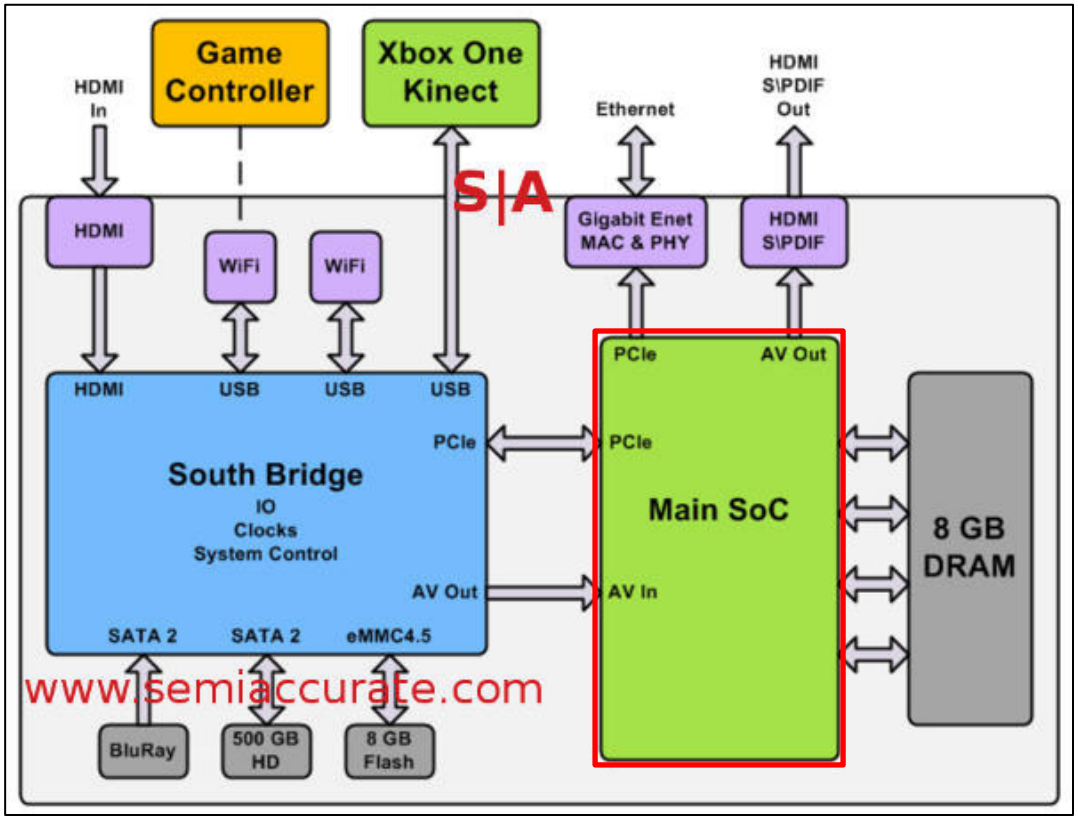
Claim Language	Infringement Evidence
	 https://semiaccurate.com/2013/08/29/a-deep-dive-into-microsofts-xbox-ones-architecture/ (annotations added). Each model of Xbox One includes a semi-custom, single-chip CPU/GPU.

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SPEC	XBOX ONE X	XBOX ONE S	XBOX ONE
Dimensions	30cm x 24cm x 6cm	29.5cm x 23cm x 6.5cm	34.3cm x 26.3cm 8cm
Weight	8.4lbs	6.4lbs	7.8lbs
CPU	Custom CPU @ 2.3 GHz, 8 cores	Custom Jaguar CPU @ 1.75GHz, 8 cores	Custom Jaguar CPU @ 1.75GHz, 8 cores
GPU	Custom GPU @ 1.172 GHz, 40 CUs, Polaris features, 6.0 TFLOPS	Custom GPU @ 914 MHz, 12 CUs, 1.4 TFLOPS	Custom GPU @ 853 MHz, 12 CUs, 1.3 TFLOPS
Memory	12 GB GDDR5 @ 326 GB/s	8 GB DDR3 @ 68 GB/s, 32 MB ESRAM @ 218 GB/s	8 GB DDR3 @ 68 GB/s, 32 MB ESRAM @ 204 GB/s
Flash	8GB	8GB	8GB
Internal Storage	1TB HDD	500GB, 1TB, 2TB HDD	500GB, 1TB HDD
Optical Disc Drive	4K UHD Blu-ray	4K UHD Blu-ray	Blu-ray
PSU	245W, Internal	120W, Internal	220W, External

https://news.xbox.com/en-us/wp-content/uploads/sites/2/Xbox_One_Spec_Sheet.pdf (annotations added).

The functionality of each processor, across Xbox One models, is identical in relevant part.

The processor in each Xbox One model contains an integrated central processing unit, interface controller and PLL clock circuitry in a single chip. As shown below, the processor (labeled "Main SoC") includes at least two PCIe interfaces on-chip: one for connecting to the southbridge and one for connecting to the Ethernet port via the Gigabit Ethernet MAC & PHY.

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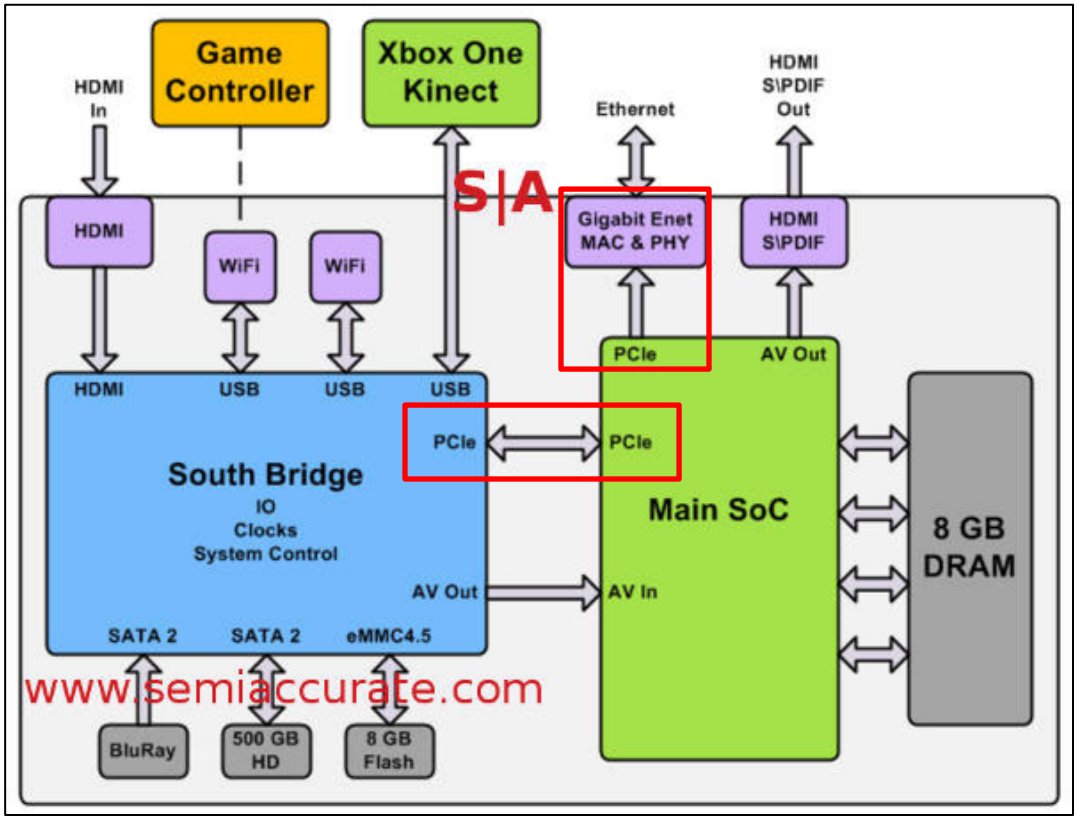
Claim Language	Infringement Evidence
	 https://semiaccurate.com/2013/08/29/a-deep-dive-into-microsofts-xbox-ones-architecture/ (annotations added). Because the processor supports on-chip PCIe, it necessarily contains one or more logic blocks to implement the PCIe functionality, i.e., a PCIe controller and related circuitry found in the Physical Layer (PHY). This logic block (or plurality of logic blocks) is, and/or is part of, an "interface

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	controller" within the meaning of this limitation. ACQIS does not possess specific information regarding the specific PCIe controller(s) and PHY(s) used in the Xbox One models or their respective processors. ACQIS reserves the right to supplement and/or amend its contentions to provide further specificity based on information obtained in discovery. As discussed below with respect to limitation [1.c], the processor, e.g., the X887732-001, includes PLL clock circuitry, including at least in the PHY(s) associated with the PCIe controller(s).
[1.b] a Low Voltage Differential Signal (LVDS) channel directly extending from the interface controller to convey address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in a serial form, wherein the first LVDS channel comprises a first unidirectional, differential signal pair to convey data in a first direction and a second unidirectional, differential signal pair to convey data in a second, opposite direction; and	The processor found in the Xbox One, e.g., the X887732-001, which includes an integrated CPU, interface controller and PLL clock circuitry, has a Low Voltage Differential Signal (LVDS) channel directly extending from the interface controller. As discussed above with respect to limitation [1.a], the processor includes on-chip PCIe interfaces, as shown below.

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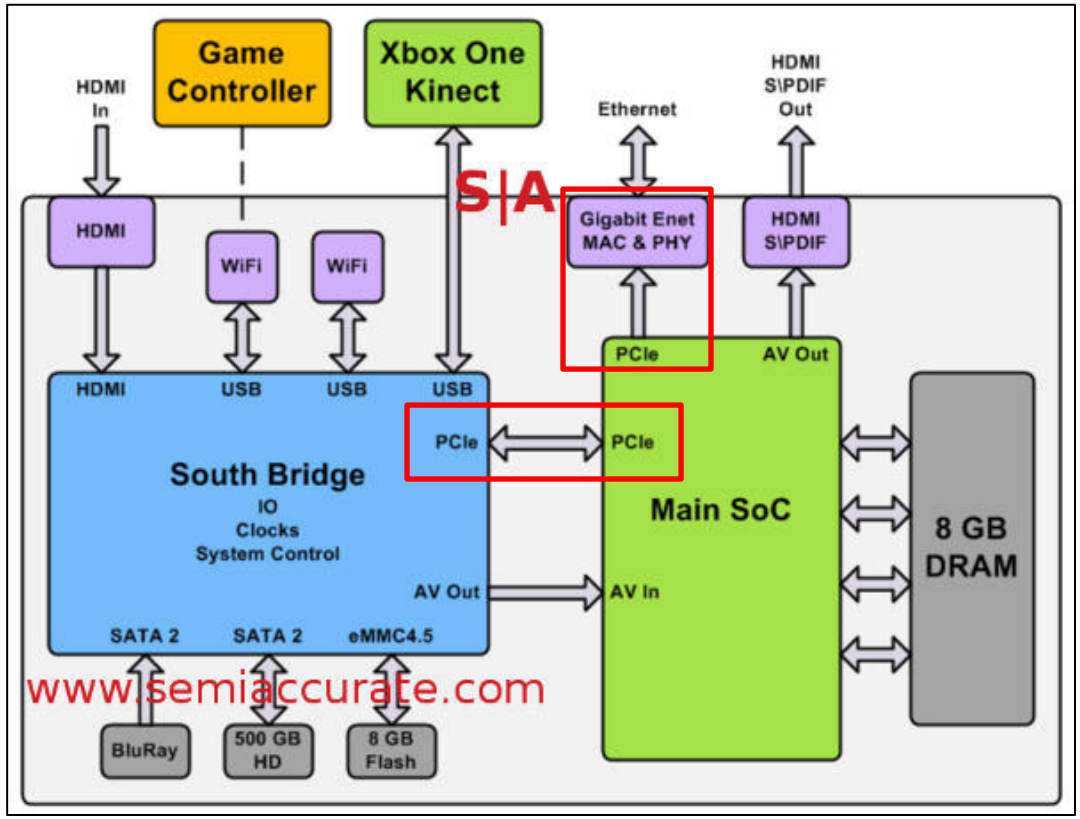
Claim Language	Infringement Evidence
	 https://semiaccurate.com/2013/08/29/a-deep-dive-into-microsofts-xbox-ones-architecture/ (annotations added). The Xbox One uses one of the processor's on-chip PCIe I/O for directly connecting the southbridge to the processor chip, as shown above. The southbridge in the Xbox One is the X861949-005, as shown below.

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Claim Language	Infringement Evidence
	 Teardown photograph of southbridge from Xbox One. The processor chip and southbridge are connected via a multi-lane PCIe implementation, likely x8, as indicated by the plurality of wire-pair traces connecting the processor chip and the southbridge chip, as shown below.

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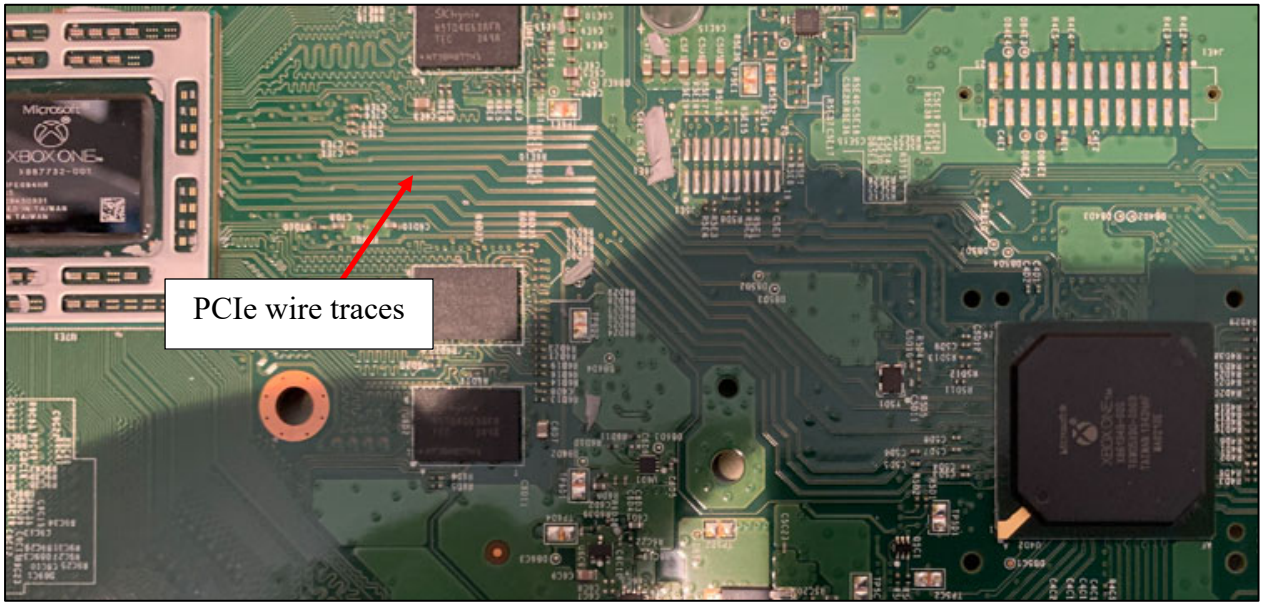
Claim Language	Infringement Evidence
	 Teardown photograph of processor-to-southbridge connection from Xbox One (annotations added). The Xbox One also uses another of the processor's on-chip PCIe I/O for directly connecting the processor chip to the Ethernet port via the Gigabit Ethernet MAC & PHY, as shown above. Each of these PCIe interfaces in the Xbox One has an LVDS channel directly extending from the interface controller that conveys address and data bits of a PCI bus transaction in a serial form. As discussed above with respect to limitation [1.a], the processor contains one or more logic blocks to implement the PCIe functionality, i.e., a PCIe controller and related circuitry found in the Physical Layer (PHY). The PCIe controller has an associated PHY connected to it via the PIPE interface. ACQIS does not possess specific information regarding the specific PCIe controller(s) and PHY(s)

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Claim Language	Infringement Evidence
	used in the Xbox One or in the processor. ACQIS reserves the right to supplement and/or amend its contentions to provide further specificity based on information obtained in discovery. LVDS is central to PCIe, providing the physical transmission medium, and all implementations of PCIe utilize LVDS: > PCI Express . . . is a serial bus which uses two low-voltage differential LVDS pairs, at 2.5Gb/s in each direction [one transmit, and one receive pair]. A PCI Express link is comprised of these two unidirectional differential pairs each operating at 2.5Gbps to achieve a basic [overall] throughput of 5Gbps [before accounting for over-head]. http://www.interfacebus.com/PCI-Express-Bus-PCIe-Description.html. Each of these LVDS channels comprises a first unidirectional, differential signal pair to convey data in a first direction and a second unidirectional, differential signal pair to convey data in a second, opposite direction. As shown in the exemplary PCIe illustrations below, each lane in a PCIe implementation contains a first unidirectional, differential signal pair to convey data in a first direction (i.e., the Tx pairs in the upper illustration and the signal pairs in red in the lower illustration) and a second unidirectional, differential signal pair to convey data in a second direction (i.e., the Rx signal pairs in the upper illustration and the signal pairs in yellow in the lower illustration). In a multi-lane PCIe configuration, the stream of bytes that make up a TLP go through byte striping, which distributes the bytes across the available lanes for serialization. *See* PCI Express Base Specification, Revision 3.0 (Nov. 10, 2010) at 195-198. The transaction's byte-oriented data (character) is encoded, serialized, and output one byte at a time per lane in the PCIe link. *Id.* Thus in PCIe, the TLP is in serial form for all link widths. *Id.*

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	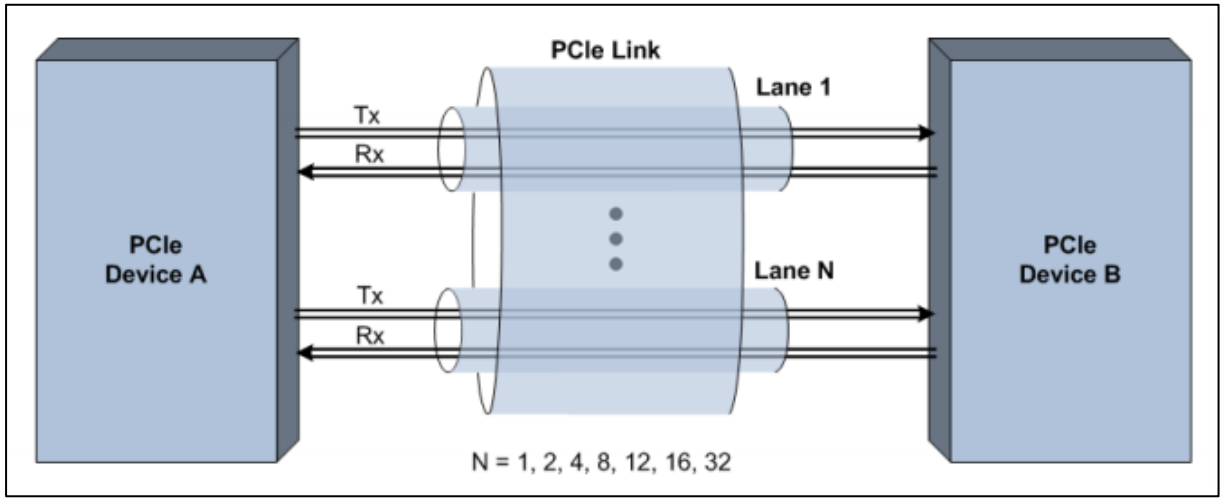 *Silicon Labs AN562, PCI Express 3.1 Jitter Requirements* (Rev. 0.2 11/15) (available at https://www.silabs.com/documents/public/application-notes/AN562.pdf), at 2.

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	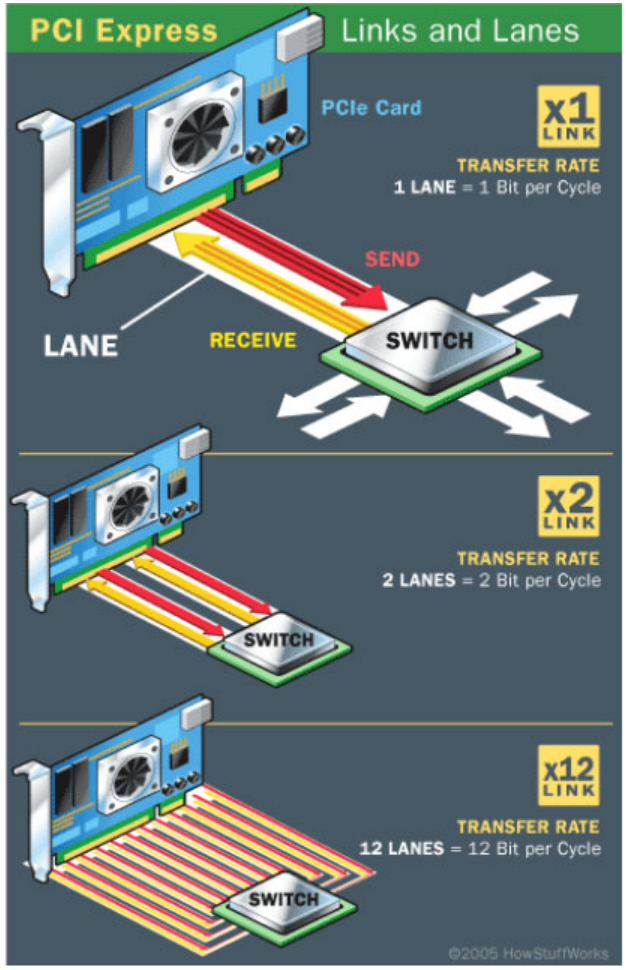 https://computer.howstuffworks.com/pci-express.htm.

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	The data that is transmitted in a serial PCIe bus transaction includes address and data bits of a PCI bus transaction. The transaction layer packets (TLPs) used for PCIe data transmission include both address and data bits of a PCI bus transaction. **The Address Element** The address elements of the TLP provide the address to select specific bytes within the memory and I/O address spaces. The address elements also provide the ID Routing and the register address to select the specific bytes of the configuration register block in the configuration address space. Finally, address elements also provide the ID and Implied Routing for the message address space. *Header field of TLP contains:* **ADDRESS:** The "typical" address bits for memory and I/O address space. The address can also be used in message vendor-defined transaction packets. *The Complete PCI Express Reference*, Intel Press (2003), at 218. **The Data Element** The data element of the transaction packet provides the actual data being accessed. *The Complete PCI Express Reference*, Intel Press (2003), at 220.

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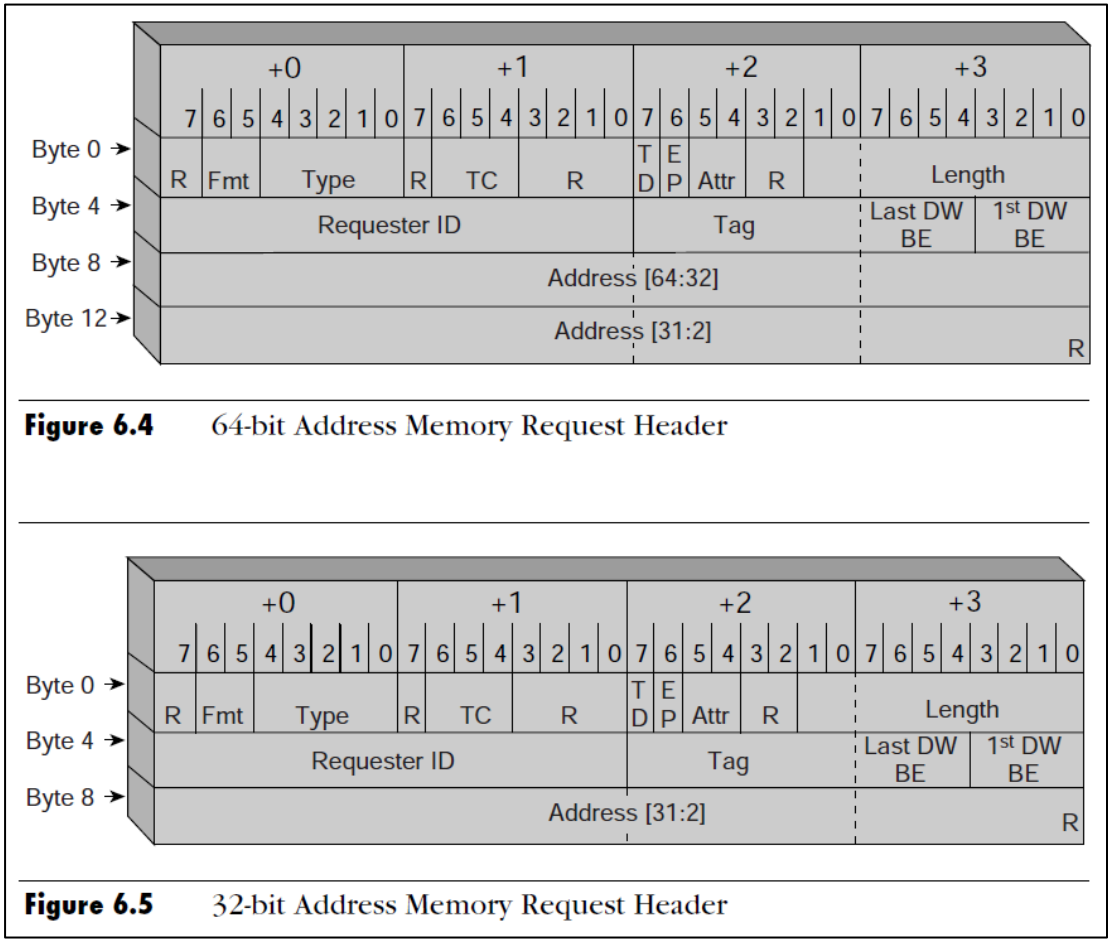

Figure 6.4 64-bit Address Memory Request Header

Figure 6.5 32-bit Address Memory Request Header

Introduction to PCI Express – A Hardware and Software Developers Guide, Intel Press (2003), at 100.

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	Further, PCIe is backwards compatible with PCI, as PCI is described in the PCI Local Bus Specification. In PCIe, "[k]ey PCI attributes, such as its usage model, load-store architecture, and software interfaces, are maintained, whereas its parallel bus implementation is replaced by a highly scalable, fully serial interface." PCI Express Base Specification, Revision 3.0 (Nov. 10, 2010) ("PCIe 3.0 Spec.") at 37. PCIe maintains a "PCI compatible software model," providing: ❑ **PCI compatible software model:** • Ability to enumerate and configure PCI Express hardware using PCI system configuration software implementations with no modifications • Ability to boot existing operating systems with no modifications • Ability to support existing I/O device drivers with no modifications • Ability to configure/enable new PCI Express functionality by adopting the PCI configuration paradigm PCIe 3.0 Spec. at 38. A Peripheral Component Interconnect (PCI) bus transaction, in accordance with the industry standard PCI Local Bus Specification, Revision 2.2 (Dec. 18, 1998) ("*PCI Specification*"), for communication with an interconnected peripheral component (a "PCI transaction") consists of an address phase and one or more data phases. (*See, e.g.*, *PCI Specification* at 9, 301.) Example transactions include input/output (I/O) read, I/O write, memory read, memory write, configuration read, and configuration write. (*See, e.g.*, *PCI Specification* at 21-23.) A PCI transaction facilitates communication and data transfer among computer components, such as processors, memory, and peripheral devices. (*See, e.g.*, *PCI Specification* at 1, 3.) PCI transactions include a set of address bits, a set of data bits, a set of command bits, and a set of byte enable information bits. (*See, e.g.*, *PCI Specification* at 9-10.) The

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	address bits allow one component to communicate with another specific component. (*See, e.g.*, *PCI Specification* at 9, 27-29.) The data bits transfer data from one component to another. (*See, e.g.*, *PCI Specification* at 9.) The command bits indicate the type of transaction (such as memory, I/O, or configuration) and control the transaction. (*See, e.g.*, *PCI Specification* at 21-24.) The byte enable information bits indicate the size of the data transfer and the bytes in the data transfer that contain valid data. (*See, e.g.*, *PCI Specification* at 10, 28.) The PCI Express™ (PCIe) Base Specification Revision 1.0a (Apr. 15, 2003) ("*PCIe Specification*"), utilizes transactions to facilitate communication and data transfer among computer components. (*See, e.g.*, *PCIe Specification* at 27.) PCIe transactions are defined in the PCIe Transaction Layer. (*See, e.g.*, *PCIe Specification* at 36.) PCIe transactions include read and write transactions. (*See, e.g.*, *PCIe Specification* at 42.) PCIe transactions are communicated using bits. (*See, e.g.*, *PCIe Specification* at 44.) PCIe employs the three transaction types (memory, I/O, and configuration) described in the PCI Local Bus Specification. (*See, e.g.*, *PCIe Specification* at 36, 45.) PCIe provides a PCI-compatible software model. (*See, e.g.*, *PCIe Specification* at 27.) PCIe transactions include command bits to indicate the type of transaction (such as memory, I/O, or configuration) and control the transaction. (*See, e.g.*, *PCIe Specification* at 44-47.) PCIe transactions include address bits to allow one component to communicate with another specific component. (*See, e.g.*, *PCIe Specification* at 49-50; *see also, e.g.*, *The Complete PCI Express Reference*, Intel Press (2003), at 218.) PCIe transactions include data bits to transfer data between components. (*See, e.g.*, *PCIe Specification* at 44; *see also, e.g.*, *The Complete PCI Express Reference*, Intel Press (2003), at 220.) PCIe transactions include byte enable information to indicate the size of the data transfer and the bytes in the data transfer that contain valid data. (*See, e.g.*, *PCIe Specification* at 52-53; *see also, e.g.*, *Introduction to PCI Express – A Hardware and Software Developers Guide*, Intel Press (2003), at 100.) A PCIe transaction therefore provides a Peripheral Component Interconnect (PCI) bus transaction in accordance with the industry standard PCI Local Bus Specification, for communication with an

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	interconnected peripheral component. A PCIe transaction provides address bits, data bits, and byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction. To the extent that Microsoft contends that a PCIe transaction does not provide a Peripheral Component Interconnect (PCI) bus transaction or address bits, data bits, and/or byte enable information bits of a Peripheral Component Interconnect (PCI) bus transaction, a PCIe transaction satisfies these claim elements under the doctrine of equivalents. A PCIe transaction—including its address, data, and byte enable information bits—performs substantially the same function, in substantially the same way, to obtain the same result as a PCI transaction, including its address, data, and byte enable information bits. A PCIe transaction—including its address, data, and byte enable information bits—is not substantially different from a PCI transaction, including its address, data, and byte enable information bits. A PCI transaction and a PCIe transaction both perform the function of facilitating communication among components in a computer system. A PCI transaction and a PCIe transaction perform this function by utilizing address bits, data bits, and byte enable bits. In both PCI and PCIe transactions, address bits allow one component to communicate with another specific component. In both PCI and PCIe transactions, data bits transfer data from one component to another. In both PCI and PCIe transactions, command bits indicate the type of transaction and control the transaction. In both PCI and PCIe transactions, byte enable bits indicate the size of the data transfer and the bytes in the data transfer that contain valid data. A PCI transaction and a PCIe transaction therefore both perform the function of facilitating communication among components in a computer system in substantially the same way. The address bits, data bits, command bits, and byte enable information bits in a PCIe transaction do not differ substantially from the address bits, data bits, command bits, and byte enable information bits in a PCI transaction. A PCIe transaction uses substantially similar bits as a PCI transaction in order to maintain consistency and software compatibility with PCI. A PCI transaction and a PCIe transaction produce the same result of communication among components in a computer system.

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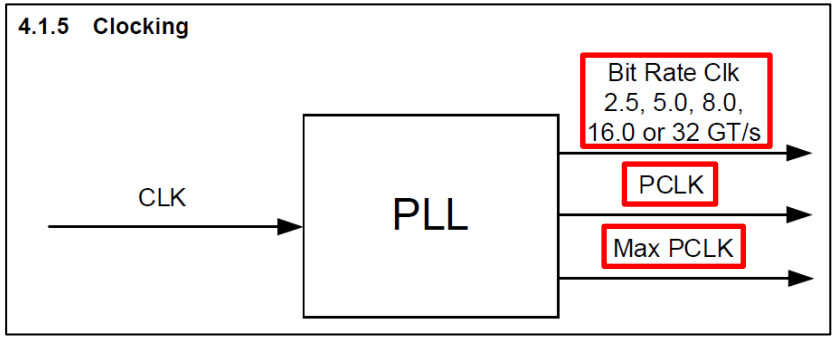
[1.c] wherein the PLL clock circuitry generates different clock frequencies, and the interface controller conveys the PCI bus transaction through the LVDS channel based on the different clock frequencies.	As discussed above with respect to limitation [1.a], the processor in each model of Xbox One, e.g., the X887732-001 processor, includes an on-chip PCIe controller and an associated PHY for each PCIe interface. The PHY(s) in the processor, e.g., the X887732-001 processor in the Xbox One, includes PLL clock circuitry. Each PHY contains at least one PLL and likely contains multiple PLLs. Within the PHY Interface for the PCI Express Architecture (PIPE), the PLL clock circuitry generates at least two clocks at different frequencies. One frequency is used as a bitrate clock (2.5 GHz – 32 GHz, depending on the PCIe transfer rates supported; PCIe 3.x supports 8 GT/s, and PCIe 2.x supports 5 GT/s), and the other is for the PIPE interface to the rest of the PCIe controller, i.e., PCLK (or pipe_clock) at 125 MHz or 250 MHz. Additionally, the PLL clock circuitry may generate a third clock frequency which is the bitrate clock divided by 10, i.e., bit rate clk / 10. Thus, the PLL clock circuitry generates different clock frequencies, which are used to convey the PCI bus transactions through the LVDS channel.  *PHY Interface for the PCI Express, SATA, USB 3.1, DisplayPort, and Converged IO Architectures*, Version 5.1 (2018) (available at https://www.intel.com/content/dam/www/public/us/en/documents /white-papers/phy-interface-pci-express-sata-usb30-architectures-3.1.pdf), at 32 (annotations added).

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	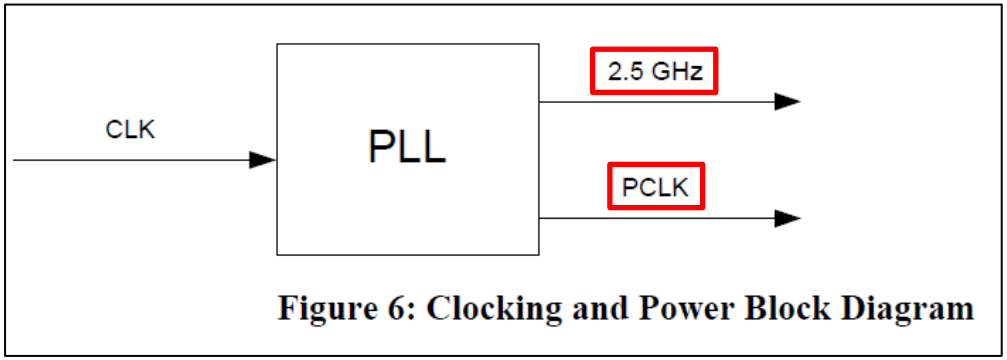 **Figure 6: Clocking and Power Block Diagram** *PHY Interface for the PCI Express Architecture*, Version 2.00 (2007) (available at http://www.applistar.com/wp-content/uploads/apps/pipe2_00.pdf), at 11 (annotations added).

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	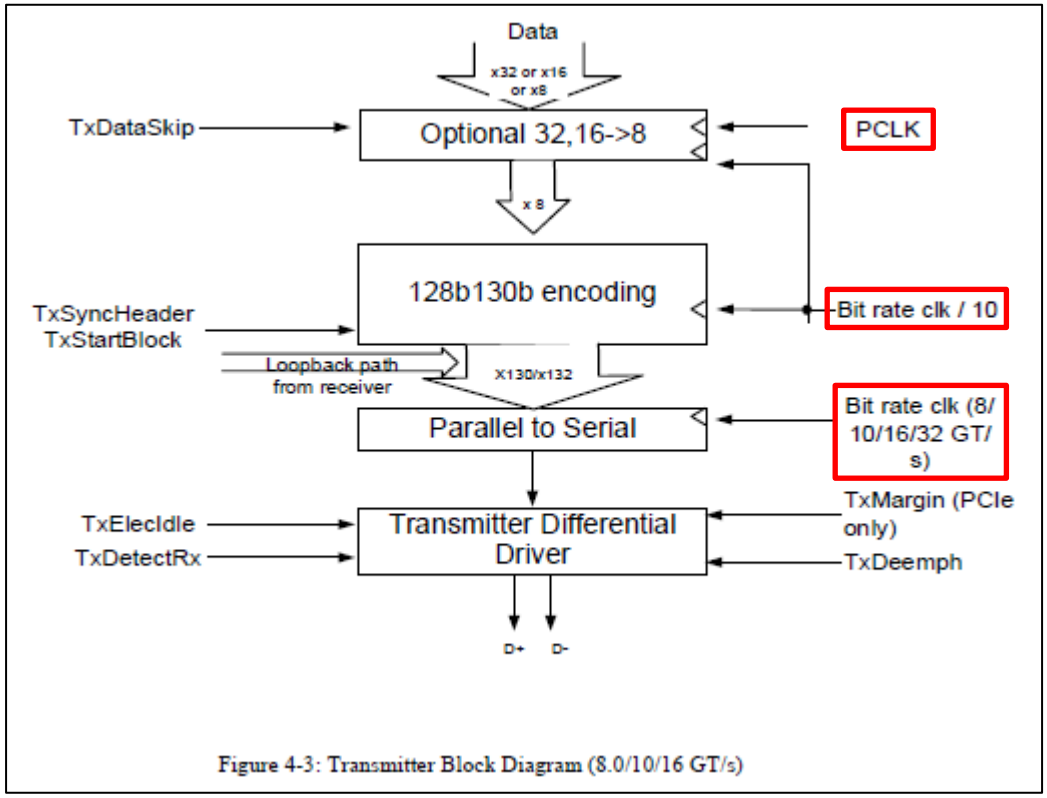 Figure 4-3: Transmitter Block Diagram (8.0/10/16 GT/s) *PHY Interface for the PCI Express, SATA, USB 3.1, DisplayPort, and Converged IO Architectures*, Version 5.1 (2018) (available at https://www.intel.com/content/dam/www/public/us/en/documents /white-papers/phy-interface-pci-express-sata-usb30-architectures-3.1.pdf), at 29 (annotations added).

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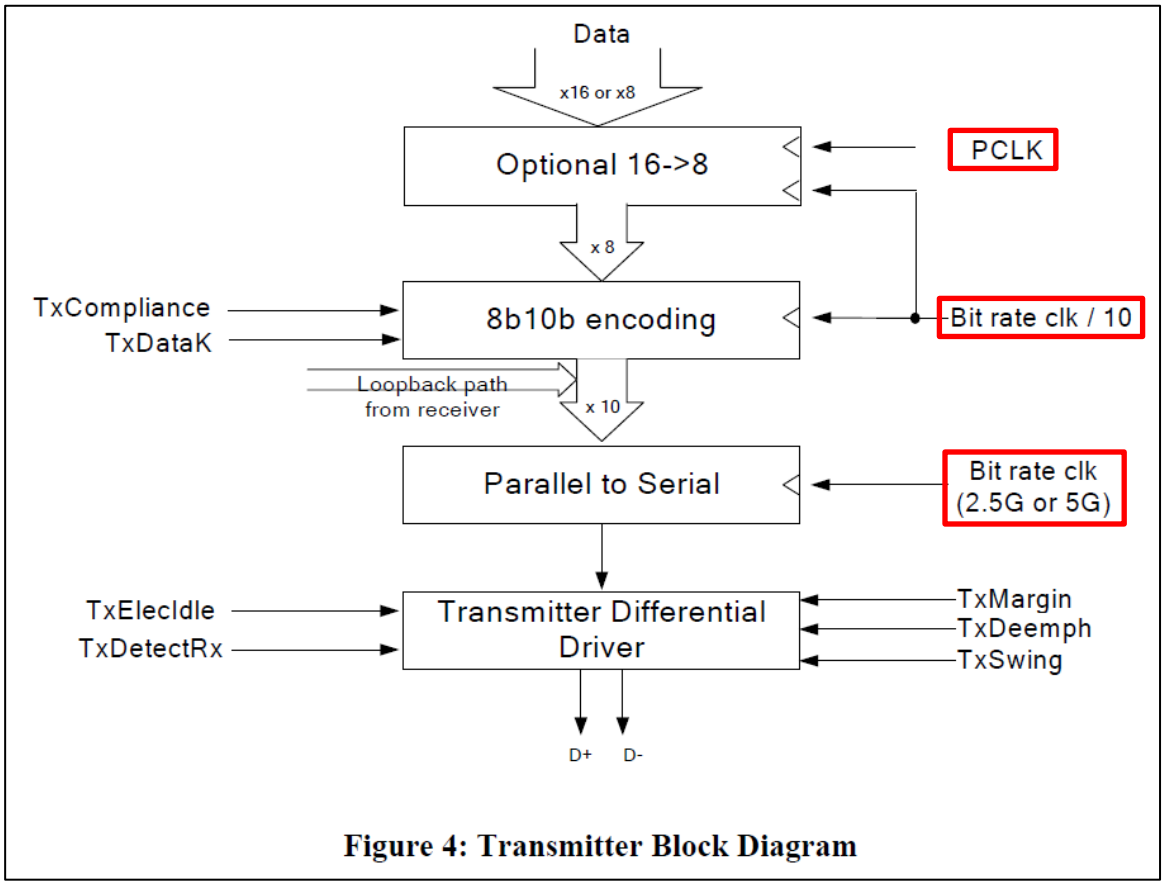
Claim Language	Infringement Evidence
	 **Figure 4: Transmitter Block Diagram** *PHY Interface for the PCI Express Architecture*, Version 2.00 (2007) (available at http://www.applistar.com/wp-content/uploads/apps/pipe2_00.pdf), at 10 (annotations added).

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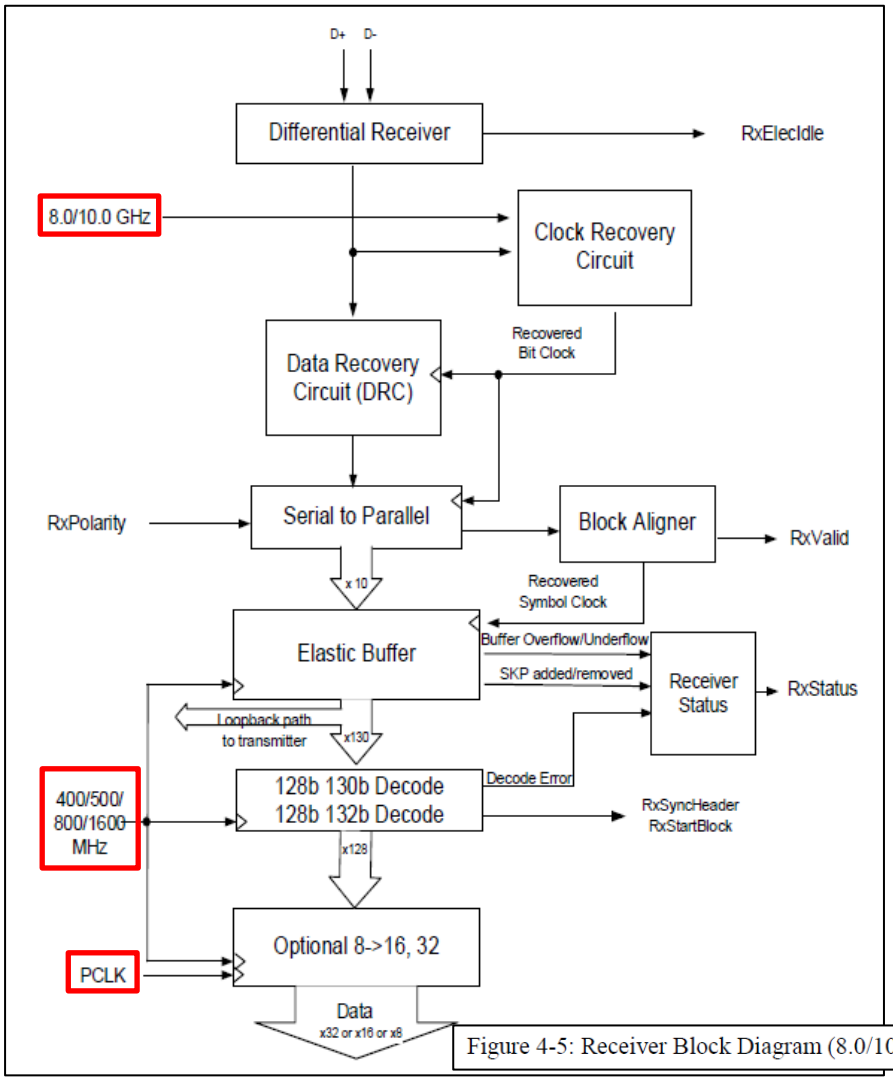
Claim Language	Infringement Evidence
	 Figure 4-5: Receiver Block Diagram (8.0/10/16 GT/s)

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Claim Language	Infringement Evidence
	PHY Interface for the PCI Express, SATA, USB 3.1, DisplayPort, and Converged IO Architectures, Version 5.1 (2018) (available at https://www.intel.com/content/dam/www/public/us/en/documents/white-papers/phy-interface-pci-express-sata-usb30-architectures-3.1.pdf), at 31-32 (annotations added).

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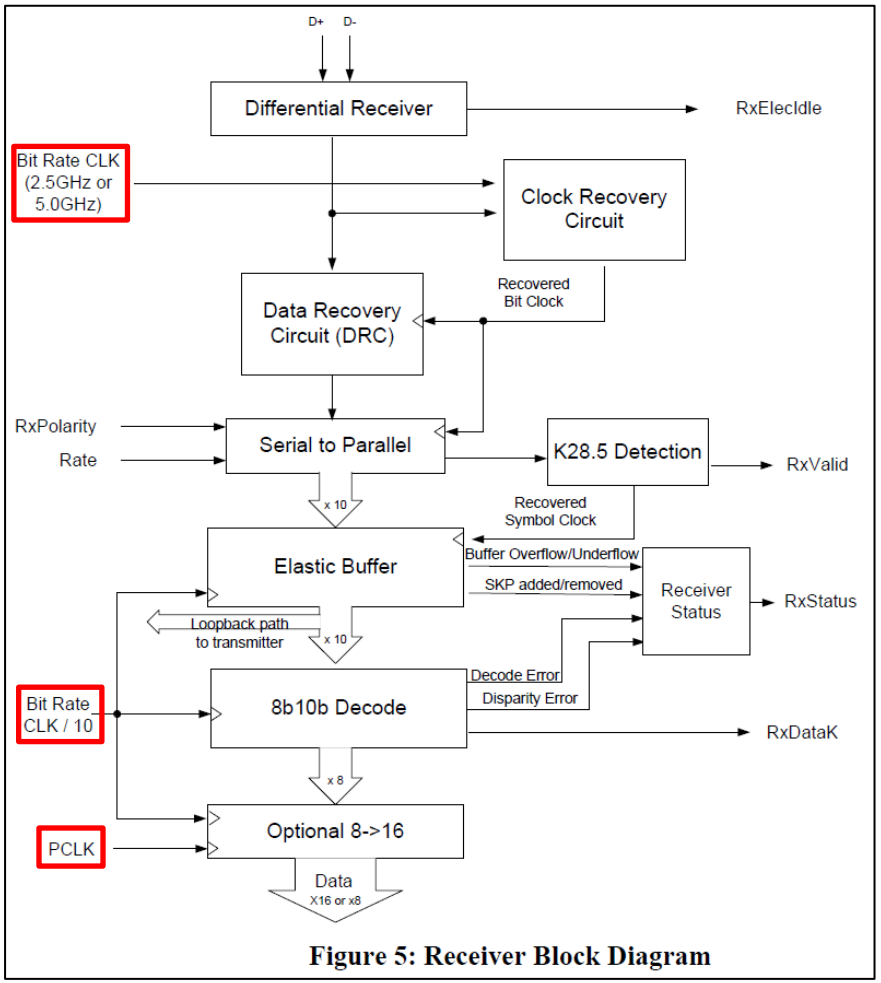
Claim Language	Infringement Evidence
	 **Figure 5: Receiver Block Diagram**

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PHY Interface for the PCI Express Architecture, Version 2.00 (2007) (available at http://www.applistar.com/wp-content/uploads/apps/pipe2_00.pdf), at 11 (annotations added).

Table 6-18. External Input Signals
<table>
<tr><th>Name</th><th>Active Level</th><th>Description</th><th>Relevant Protocols</th></tr>
<tr><td>CLK</td><td>Edge</td><td>This differential Input is used to generate the bit-rate clock for the PHY transmitter and receiver. Specs for this clock signal (frequency, jitter, …) are implementation dependent and must be specified for each implementation. This clock may have a spread spectrum modulation.</td><td>PCIe, SATA, USB, DisplayPort, Converged IO</td></tr>
<tr><td>PCLK</td><td>Rising Edge</td><td>This signal is relevant for "PCLK as PHY Input" mode only.

All data movement across the parallel interface is synchronized to this clock. This clock operates at a frequency set by PCLK Rate. The rising edge of the clock is the reference for all signals. Spread spectrum modulation on this clock is allowed.</td><td>PCIe, SATA, USB, DisplayPort, Converged IO</td></tr>
</table>

PHY Interface for the PCI Express, SATA, USB 3.1, DisplayPort, and Converged IO Architectures, Version 5.1 (2018) (available at https://www.intel.com/content/dam/www/public/us/en/documents/white-papers/phy-interface-pci-express-sata-usb30-architectures-3.1.pdf), at 77.
</td></tr>
</table>

Exhibit B-1
ACQIS's Preliminary Infringement Contentions for U.S. Patent No. 9,529,768
Microsoft Xbox One

<table>
<tr><th>Claim Language</th><th>Infringement Evidence</th></tr>
<tr><td></td><td>
<table>
<tr><th>Name</th><th>Direction</th><th>Active Level</th><th>Description</th></tr>
<tr><td>CLK</td><td>Input</td><td>Edge</td><td>This Input is used to generate the bit-rate clock for the PHY transmitter and receiver. Specs for this clock signal (frequency, jitter, …) are implementation dependent and must be specified for each implementation. This clock may have a spread spectrum modulation.</td></tr>
<tr><td>PCLK</td><td>Output</td><td>Rising Edge</td><td>Parallel interface data clock. All data movement across the parallel interface is synchronized to this clock. This clock operates at 125MHz, 250MHz, or 500 MHz depending on the Rate control input and the data interface width. The rising edge of the clock is the reference for all signals. Spread spectrum modulation on this clock is allowed.</td></tr>
</table>

PHY Interface for the PCI Express Architecture, Version 2.00 (2007) (available at http://www.applistar.com/wp-content/uploads/apps/pipe2_00.pdf), at 16.

Additionally, PLLs are often used within the PCIe PHY as part of the clock and data recovery (CDR) functionality of the receiver.
</td></tr>
</table>

Exhibit B-1
ACQIS's Preliminary Infringement Contentions for U.S. Patent No. 9,529,768
Microsoft Xbox One

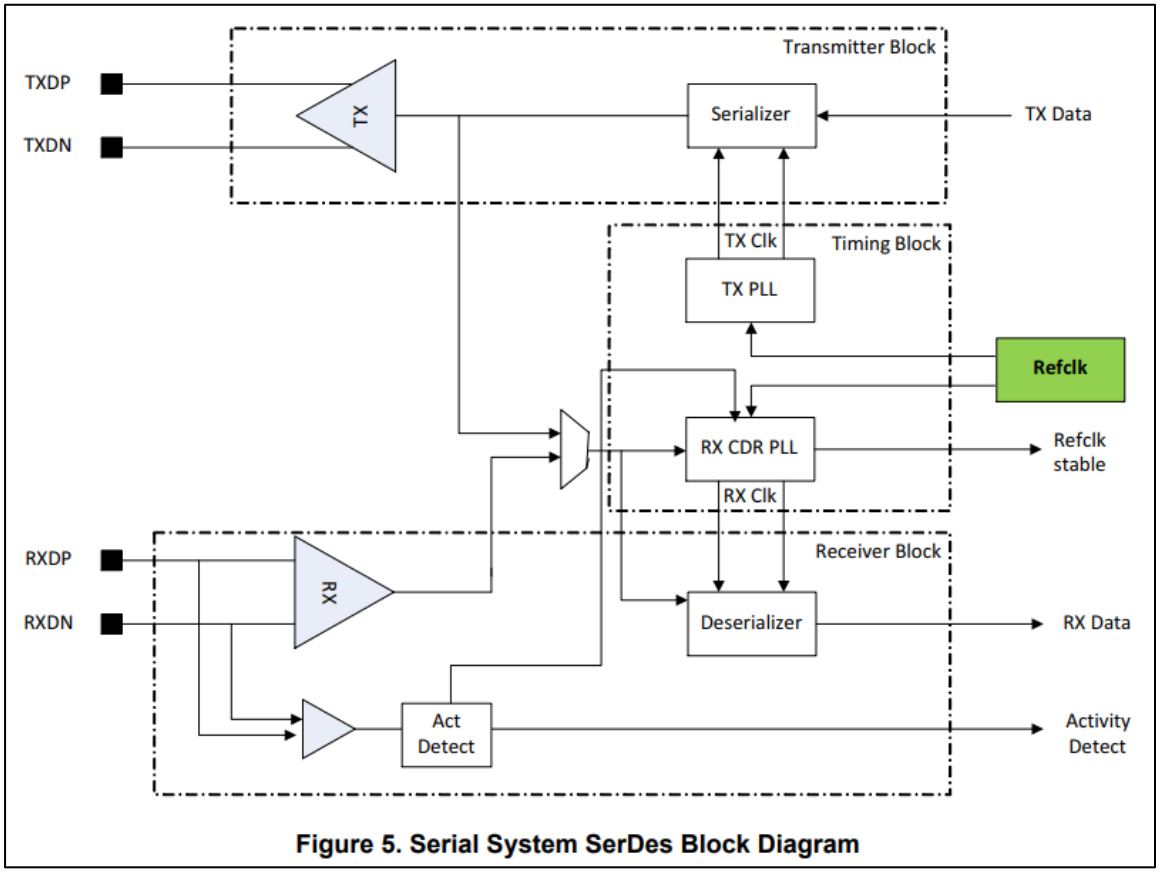
Claim Language	Infringement Evidence
	 **Figure 5. Serial System SerDes Block Diagram** *A System Designer's Guide for Building a PCIe Clock Tree while Addressing Timing Challenges*, Application Note AND9202/D, ON Semiconductor (available at https://www.onsemi.com/pub/Collateral/AND9202-D.PDF), at 5.

Exhibit B-1
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Microsoft Xbox One

Claim Language	Infringement Evidence
	The PLL clock circuitry in each PCIe PHY in the processor also generates different clock frequencies based on PCIe version and the associated data transfer rate. The PLL clock circuitry, e.g., the transmit (TX) PLL, multiplies the reference clock frequency to achieve the desired data rate. This standard approach is consistent with the discussion below. **3. Refclk and Clocking Architectures** An external clock reference clock (Refclk) is required for transmitting data between two PCIe devices. A Refclk frequency of 100 MHz ±300 ppm is specified for all three line rates (2.5 Gbps, 5.0 Gbps, 8.0 Gbps). The burden has been placed on the TX PLL to multiply the 100 MHz Refclk frequency to the desired data rate. Although the Refclk frequency has remained the same, the jitter performance requirements of the Refclk have improved to support the higher data rates prevalent with PCI Express 2.1 and 3.1. We will look at the Refclk jitter requirements in the following sections. *Silicon Labs AN562, PCI Express 3.1 Jitter Requirements* (Rev. 0.2 11/15) (available at https://www.silabs.com/documents/public/application-notes/AN562.pdf), at 3. The interface controller(s) in the processor, e.g., the X887732-001 processor in the Xbox One, thus conveys the PCI bus transaction through the LVDS channel based on different clock frequencies.
2. The computer of claim 1 wherein the interface controller conveys the PCI bus transaction through the LVDS channel based on a selected frequency of the different clock frequencies.	*See* claim 1, above. The interface controller in the processor in the Xbox One, e.g., the X887732-001 processor, conveys the PCI bus transaction through the LVDS channel based on a selected frequency of the different clock frequencies. The PLL within the PCIe PHY will select one bit rate frequency based on the version of the PCIe protocol and the highest common data rate used for the link.